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10/020,019	12/07/2001	Francesco Pessolano	NL 000667	8972

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EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/020,019	PESSOLANO ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --.

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-11,13 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-11,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 5-11 and 13-14 are pending.

2. The office acknowledges the following papers:

Claims and arguments filed on 5/7/2007.

Withdrawn Rejections

3. The claim objection for claim 5 is withdrawn due to amendment.

New Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 3 are rejected under 35 U.S.C. §103(a) as being unpatentable over White et al. (U.S. 5,632,023).

6. As per claim 3:

White disclosed a digital signal processing apparatus for executing a plurality of operations in a loop (It's obvious to one of ordinary skill in the art that a processor can execute instructions that are in or out or a loop), comprising a plurality of functional units wherein each functional unit is adapted to execute operations (White: Figure 2b elements 235, 240, 245, 260 and 265), and respective control means for said each functional unit for controlling said functional units in coordination with one another

(White: Figure 2b elements 235R, 240R, 245R, 260R and 265R, column 11 lines 36-47)(Each reservation station receives decoded operations from the Decode Unit and issues the instructions to its associated functional unit when all operands are available, thereby controlling its function.) in response to a single fetch unit (White: Figure 2a element 230) and a single decode unit (White: Figure 2A element 205), characterized by FIFO (first-in/first-out) register means adapted for supporting data-flow communication among said functional units (White: Figure 2a element 285, column 11 lines 21-22)(The Reorder Buffer is a FIFO register (register meaning a device capable of retaining information of the aggregate information in a digital computer) device which is utilized by all of the functional units to support data-flow, in that the functional units can use the data before it is committed to the register file. White explicitly states the Reorder Buffer is a FIFO buffer, "Reorder buffer 285 is managed as a first-in first-out (FIFO) device."), wherein said functional units transfer control to the single fetch unit upon completion of an operation included in the loop and execute instructions of a subsequent loop instead of being stalled or executing a no-operation instruction (White: Figure 2 elements 225, 230, 235, column 11 lines 63-67 continued to column 12 lines 1-9 and column 13 lines 1-15)(A branch instruction in compiled computer programs is used to end a loop. When the condition is met to end a loop, a branch could either be taken or not taken depending on the loop to exit it. Upon exiting the loop, it's obvious to one of ordinary skill in the art that execution would want to be continued as opposed to stalling or executing no-ops for the advantage of increased performance through increased throughput. The branch prediction and prefetch elements allow for

prefetching instructions at the exit of the loop. Thus, since instructions are already within the instruction cache at the exit of the loop, it's obvious to one of ordinary skill in the art that these instructions can be fetched and executed instead of stalling or executing no-ops. In addition, it's obvious to one of ordinary skill in the art that a program could execute nested loops, which results in upon exiting one loop, another loop is entered.).

7. Claims 1-3, 5-11 and 13-14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Tsushima et al. (U.S. 6,044,450).

8. As per claim 1:

Tsushima disclosed a digital signal processing apparatus for executing a plurality of operations in a loop (It's obvious to one of ordinary skill in the art that a processor can execute instructions that are in or out or a loop), comprising

A plurality of functional units wherein each functional unit is adapted to execute operations (Tsushima: Figure 1 elements 204-1, 204-2, 205-1, 205-2, 206-1, 206-2, and 207);

And control means for controlling said functional units characterized in that said control means comprises a fetch unit, a decode unit, and a plurality of control units responsive to said decode unit (Tsushima: Figures 1, 3, and 5 elements 202, 203, and 300, column 6 lines 24-53)(Instruction Fetch Unit 202, Instruction Expanding Unit 300 and Decode Unit 203 make up the control means. Small Instruction Generating Circuit 303-1 and 303-2 are in each of the Instruction Expanding Circuit (300a-d) of the

Instruction Expanding Unit 300. The Small Instruction Generating Circuits 303-1 and 303-2 receive decompressed opcodes and other control data, i.e., decoded control signals from the decode unit. While this data supplied to the Small Instruction Generating Circuits does not come from the "Decode Unit 203", the control data does come from hardware that extracts (decodes) control information/data from instructions, and thus the control data/information comes from a "Decode Unit".);

Wherein at least one control unit is operatively associated with a respective functional unit for controlling its function, including controlling a number of repetitions of execution of its function (Tsushima: Figure 5 elements 600, 604, and 620, column 10 lines 35-54 and column 16 lines 36-67 continued to column 17 lines 1-28)(Each small instruction generator contains a "NOP Instruction Register 604, Selector 600 and a Control Circuit 620, which control the function for it's respective functional unit. These elements control whether a regular instruction or a nop will be executed by the functional unit. The Small Instruction Generator chooses between the opcode provided by line 50-1 or a NOP instruction using the Selector, and thus controls the function of the functional unit. Furthermore, the Control Circuit 620 controls the number or repetitions of the execution of the NOP function.);

And each functional unit is adapted to execute operations in an autonomous manner under control of the control unit associated therewith (Tsushima: Figure 5 element 620, column 10 lines 35-54 and column 16 lines 36-67 continued to column 17 lines 1-28)(Each functional unit is autonomous under control of the Control Unit 620, as a number of NOPs is encoded and delivered to the Small Instruction Generating Circuits

and the Small Instruction Generating Circuit alone issues the appropriate number of NOP instructions.) including transfer of control to the control means upon completion of an operation included in the loop and execution of instructions of a subsequent loop instead of being stalled or executing a no-operation instruction (Figure 2 element 7)(A branch instruction in compiled computer programs is used to end a loop. When the condition is met to end a loop, a branch could either be taken or not taken depending on the loop to exit it. Upon exiting the loop, it's obvious to one of ordinary skill in the art that execution would want to be continued as opposed to stalling or executing no-ops for the advantage of increased performance through increased throughput. Official notice is given that a branch predictor with a prefetch mechanism could be added to prefetch instructions at the exit of the loop. Thus, since instructions are already within the instruction cache at the exit of the loop, it's obvious to one of ordinary skill in the art that these instructions can be fetched and executed instead of stalling or executing no-ops. In addition, it's obvious to one of ordinary skill in the art that a program could execute nested loops, which results in upon exiting one loop, another loop is entered.).

9. As per claim 2:

Tsushima disclosed an apparatus according to claim 1, characterized by FIFO (first-in/first-out) register means adapted for supporting data-flow communication among said functional units (Tsushima: Figure 3 element 300a-d, column 16 lines 27-35)[The operand queues 302-1 and 302-2 of each Instruction Expanding Circuit (300a-d) are each FIFO register means adapted for supporting data-flow communication among said functional units. From a first point of view, data flows from each queue to the

associated functional unit, which is an example of communication among functional units. From a second point of view, the opcodes sent from the queues 302-1 and 302-2 include, for instance, load instructions. Load instructions are executed by the load/store functional unit and load data from memory to registers, which other functional units then use. Therefore, one FIFO queue is supporting communication between the load/store functional unit and the other functional units.).

10. As per claim 3:

Tsushima disclosed a digital signal processing apparatus for executing a plurality of operations in a loop (It's obvious to one of ordinary skill in the art that a processor can execute instructions that are in or out or a loop), comprising a plurality of functional units wherein each functional unit is adapted to execute operations (Tsushima: Figure 1 elements 204-1, 204-2, 205-1, 205-2, 206-1, 206-2, and 207),

and control means for controlling said functional units in coordination with one another in response (Tsushima: Figure 5 elements 600, 604, and 620, column 10 lines 35-54 and column 16 lines 36-67 continued to column 17 lines 1-28)(Each small instruction generator contains a "NOP Instruction Register 604, Selector 600 and a Control Circuit 620, which control the function for it's respective functional unit. These elements control whether a regular instruction or a nop will be executed by the functional unit. The Small Instruction Generator chooses between the opcode provided by line 50-1 or a NOP instruction using the Selector, and thus controls the function of the functional unit. Furthermore, the Control Circuit 620 controls the number or

repetitions of the execution of the NOP function.) to a single fetch unit (Tsushima: Figure 1 element 202) and a single decode unit (Tsushima: Figure 1 element 203),

characterized by FIFO (first-in/first-out) register means (Tsushima: Figure 3 elements 302-1 and 302-2) adapted for supporting data-flow communication among said functional units (Tsushima: Figures 1 and 3, column 16 lines 27-35)(The operand queues 302-1 and 302-2 of each Instruction Expanding Circuit (300a-d) are each FIFO register means adapted for supporting data-flow communication among said functional units. From a first point of view, data flows from each queue to the associated functional unit, which is an example of communication among functional units. From a second point of view, the opcodes sent from the queues 302-1 and 302-2 include, for instance, load instructions. Load instructions are executed by the load/store functional unit and load data from memory to registers, which other functional units then use. Therefore, one FIFO queue is supporting communication between the load/store functional unit and the other functional units.),

Wherein said functional units transfer control to the single fetch unit upon completion of an operation included in the loop and execute instructions of a subsequent loop instead of being stalled or executing a no-operation instruction (Figure 2 element 7)(A branch instruction in compiled computer programs is used to end a loop. When the condition is met to end a loop, a branch could either be taken or not taken depending on the loop to exit it. Upon exiting the loop, it's obvious to one of ordinary skill in the art that execution would want to be continued as opposed to stalling or executing no-ops for the advantage of increased performance through increased

throughput. Official notice is given that a branch predictor with a prefetch mechanism could be added to prefetch instructions at the exit of the loop. Thus, since instructions are already within the instruction cache at the exit of the loop, it's obvious to one of ordinary skill in the art that these instructions can be fetched and executed instead of stalling or executing no-ops. In addition, it's obvious to one of ordinary skill in the art that a program could execute nested loops, which results in upon exiting one loop, another loop is entered.).

11. As per claim 5:

Tsushima disclosed an apparatus according to claim 2, characterized in that said FIFO register means comprises a plurality of FIFO registers (Tsushima: Figures 1 and 3 elements 302-1 and 302-2, column 16 lines 27-35)(The operand queues are FIFOs that are made up of registers. Since the registers are part of a FIFO queue, they are FIFO registers.).

12. As per claim 6:

Tsushima disclosed an apparatus according to claim 1, characterized in that each of said functional units are provided with at least one control unit (Tsushima: Figure 3 elements 303-1 and 303-2)(Each functional unit has an associated Small Instruction Generating Circuit.).

13. As per claim 7:

Tsushima disclosed an apparatus according to claim 1, which apparatus is adapted to form a pipeline consisting of a plurality of stages, wherein each stage comprises a functional unit (Tsushima: Figure 1)(The pipeline stages include at least a

Fetch stage, expanding stage, decode stage, execution stage (functional units) and write back stage (functional units to register file).).

14. As per claim 8:

Tsushima disclosed an apparatus according to claim 1, characterized in that for each control unit an instruction register and a counter are provided, wherein said counter indicates the number of times an instruction stored in said instruction register has to be executed by the corresponding functional unit (Tsushima: Figure 5 elements 601 and 604)(The counter indicates how many times the nop instruction has been executed.).

15. As per claim 9:

Tsushima disclosed an apparatus according to claim 1, further comprising a program memory means storing a main program, characterized in that said main program contains directives for instructing said control units (Tsushima: Figure 1 element 100 and 201)(Both Main Storage and Instruction Cache are memories that contain instructions, which is what controls the control circuit in the Control Units (Small Instruction Generating Circuits 303-1 and 303-2).).

16. As per claim 10:

The additional limitation(s) of claim 10 basically recite the additional limitation(s) of claim 1. Therefore, claim 10 is rejected for the same reason(s) as claim 1.

17. As per claim 11:

The additional limitation(s) of claim 11 basically recite the additional limitation(s) of claim 2. Therefore, claim 11 is rejected for the same reason(s) as claim 2.

18. As per claim 13:

The additional limitation(s) of claim 13 basically recite the additional limitation(s) of claim 7. Therefore, claim 13 is rejected for the same reason(s) as claim 7. Examiner also notes that each of the stages is executed by a functional unit, e.g., the fetch unit is a functional unit because it's function is performing instruction fetches.

19. As per claim 14:

The additional limitation(s) of claim 14 basically recite the additional limitation(s) of claim 8. Therefore, claim 14 is rejected for the same reason(s) as claim 8.

Response to Arguments

20. The arguments presented by Applicant in the response, received on 5/30/2007 are considered persuasive.

21. Applicant argues "White, Johnson, and Tsushima either individually or in combination failed to teach including transfer of control to the control means upon completion of an operation included in the loop and execution of instructions of a subsequent loop instead of being stalled or executing a no-operation instruction" for claim 3.

This argument is found to be persuasive for the following reason. The examiner agrees that none of the references either explicitly or inherently teaches the claimed limitation. However, a new ground of rejection has been given.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183

RICHARD L. ELLIS
PRIMARY EXAMINER